Lab 2: Design and Simulation of Sequential Logic Circuits -- Synchronous Counters

**CEG 2136 B - Computer Architecture**

**Fall 2017**

**School of Electrical Engineering and Computer Science University of Ottawa**

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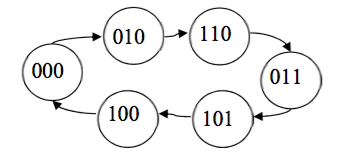
# Theoretical Part

1. **Introduction of problem**

In this lab, we created sequential circuit diagrams using various logic gates and JK Flip Flops in order to gain additional practice with the Altera DE2-115 board and the Quartus II software. This lab also introduced us to testing with an oscilloscope and allowed us to begin familiarizing ourselves with the oscilloscope.

2. **Discussion of problem**

The problem for this lab consisted of designing sequential circuits based on the state diagrams provided.



*Figure 1: A state diagram of a Modulo 6 counter*

*../../../../../../../Desktop/Screen%20Shot%202017-10-09%20at%2011.21*

*Figure 2: A state diagram of a 4-bit synchronous BCD counter*

**3. Discussion of algorithmic solution**

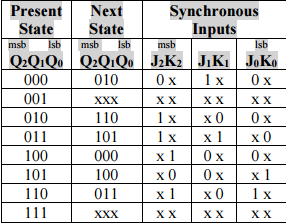
We used ANDs, NOTs and JK Flip Flops to build the sequential circuits. The diagram for part 1 contained a clock and reset inputs, three JK Flip Flops and three outputs. The diagram for part 2 contained a clock and reset inputs, four JK Flip Flops and four outputs.

# Design Part

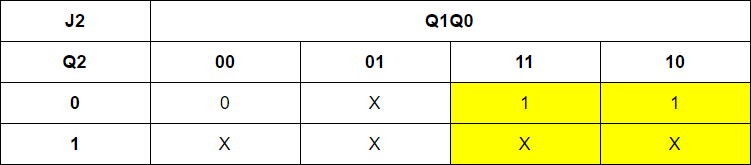
1. **Presentation of the design methodology applied to solving the lab problems**

**3 Bit Synchronous Modulo 6 Counter**

From the state diagrams, an excitation table can be made to determine the values of the inputs in the JK Flip Flops. From the values determined in the excitation table, a K-Map can be made to find the simplified equation for the input. Then using these equations, a circuit diagram can be designed.

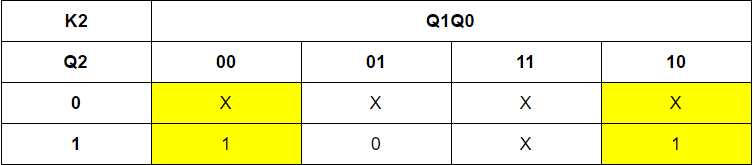
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*Table 1: The Excitation Table for the JK flip-flops Modulo 6 counter*



J2 = Q1

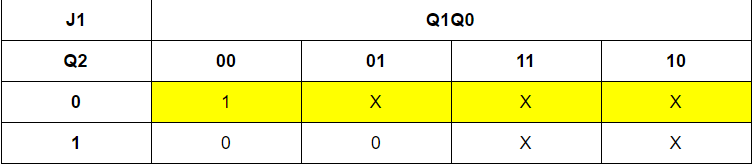
*Table 2: K-Map for J2*

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K2 = Q0’

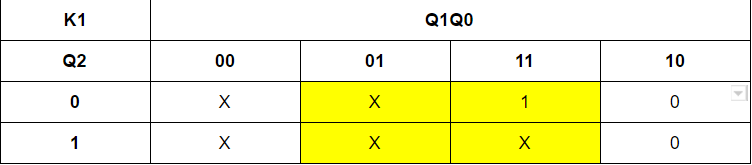
*Table 3: K-Map for K2*

*Table 4: K-Map for J1*

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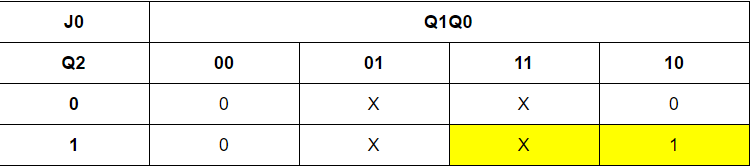
J1 = Q2’

*Table 5: K-Map for K1*

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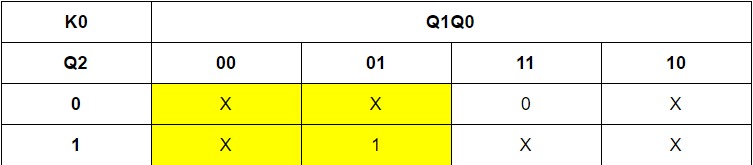
K1 = Q0

*Table 6: K-Map for J0*

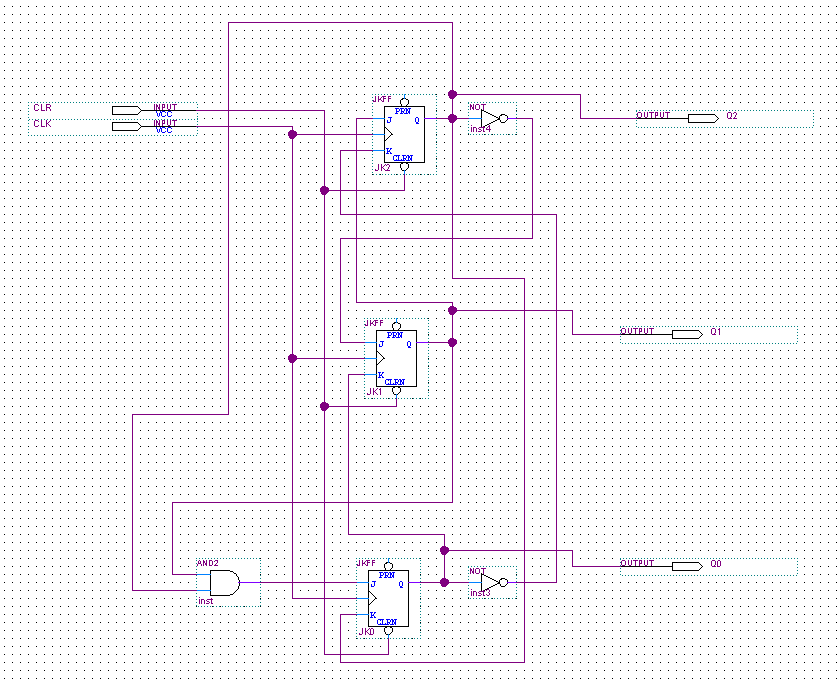
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J0 = Q1Q2

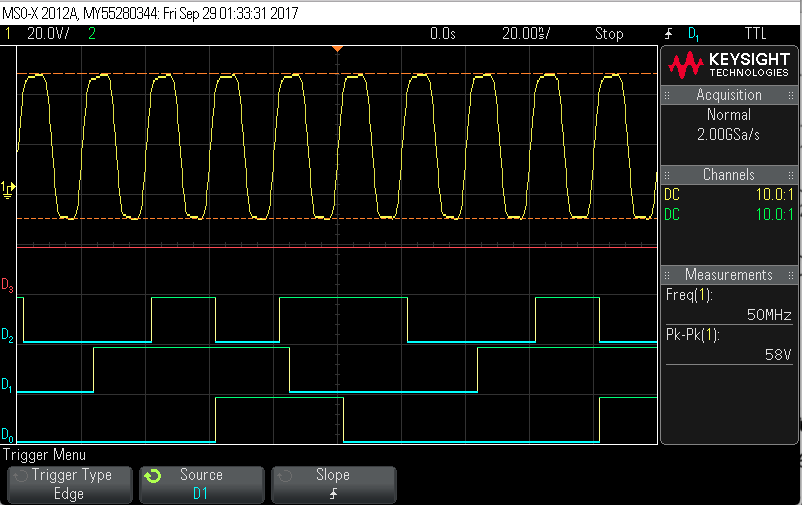
*Table 7: K-Map for K0*

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K0 = Q1’

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*Figure 1: A circuit diagram of a modulo 6 counter*



*Figure 2: Simulation of 3-bit synchronous BCD on the oscilloscop*

*Table 8: The Excitation Table for the JK flip-flops 4-bit synchronous BCD counter*

|  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- |
| Current  ABCD | Next ABCD | JAKA | JBKB | JCKC | JDKD |
| 0000 | 0001 | 0X | 0X | 0X | 1X |
| 0001 | 0010 | 0X | 0X | 1X | X1 |
| 0010 | 0011 | 0X | 0X | X0 | 1X |
| 0011 | 0100 | 0X | 1X | X1 | X1 |
| 0100 | 0101 | 0X | X0 | 0X | 1X |
| 0101 | 0110 | 0X | X0 | 1X | X1 |
| 0110 | 0111 | 0X | X0 | X0 | 1X |
| 0111 | 1000 | 1X | X1 | X1 | X1 |
| 1000 | 1001 | X0 | 0X | 0X | 1X |
| 1001 | 0000 | X1 | 0X | 0X | X1 |

*Table 9: K-Map for JA*

|  |  |  |  |  |
| --- | --- | --- | --- | --- |
| **JA** | **CD** | | | |
| **AB** | **00** | **01** | **11** | **10** |
| **00** | 0 | 0 | 0 | 0 |
| **01** | 0 | 0 | 1 | 0 |
| **11** | X | X | X | X |
| **10** | X | X | X | X |

JA = BCD

*Table 10: K-Map for KA*

|  |  |  |  |  |
| --- | --- | --- | --- | --- |
| **KA** | **CD** | | | |
| **AB** | **00** | **01** | **11** | **10** |
| **00** | x | x | x | x |
| **01** | x | x | x | x |
| **11** | x | x | x | x |
| **10** | 0 | 1 | x | x |

KA = D

*Table 11: K-Map for JB*

|  |  |  |  |  |
| --- | --- | --- | --- | --- |
| **JB** | **CD** | | | |
| **AB** | **00** | **01** | **11** | **10** |
| **00** | 0 | 0 | 1 | 0 |
| **01** | x | x | x | x |
| **11** | x | x | x | x |
| **10** | 0 | 0 | x | x |

JB = CD

*Table 12: K-Map for KB*

|  |  |  |  |  |
| --- | --- | --- | --- | --- |
| **KB** | **CD** | | | |
| **AB** | **00** | **01** | **11** | **10** |
| **00** | x | x | x | x |
| **01** | 0 | 0 | 1 | 0 |
| **11** | x | x | x | x |
| **10** | 0 | 0 | x | x |

KB = CD

*Table 13: K-Map for JC*

|  |  |  |  |  |
| --- | --- | --- | --- | --- |
| **JC** | **CD** | | | |
| **AB** | **00** | **01** | **11** | **10** |
| **00** | 0 | 1 | x | x |
| **01** | 0 | 1 | x | x |
| **11** | x | x | x | x |
| **10** | 0 | 0 | x | x |

JC = A’D

*Table 14: K-Map for KC*

|  |  |  |  |  |
| --- | --- | --- | --- | --- |
| **KC** | **CD** | | | |
| **AB** | **00** | **01** | **11** | **10** |
| **00** | x | x | 1 | 0 |
| **01** | x | x | 1 | 0 |
| **11** | x | x | x | x |
| **10** | x | x | x | x |

KC = D

*Table 15: K-Map for JD*

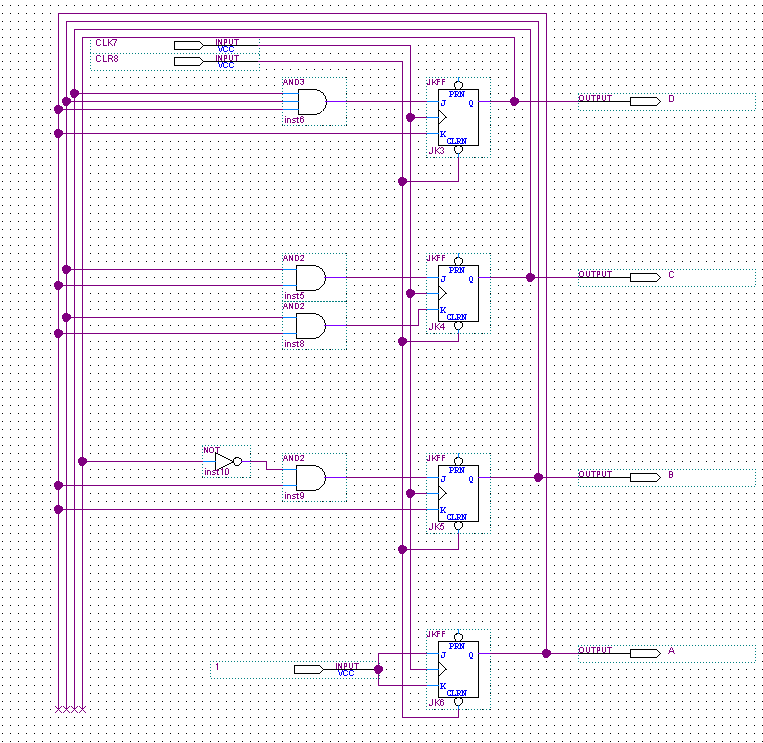
|  |  |  |  |  |
| --- | --- | --- | --- | --- |
| **JD** | **CD** | | | |
| **AB** | **00** | **01** | **11** | **10** |
| **00** | 1 | x | x | 1 |
| **01** | 1 | x | x | 1 |
| **11** | x | x | x | x |
| **10** | 1 | x | x | 1 |

JD = 1

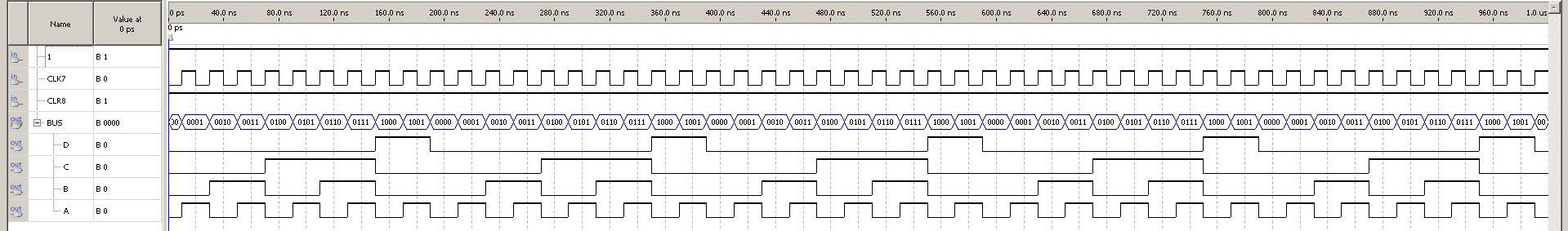
*Table 16: K-Map for KD*

|  |  |  |  |  |
| --- | --- | --- | --- | --- |
| **KD** | **CD** | | | |
| **AB** | **00** | **01** | **11** | **10** |
| **00** | x | 1 | 1 | x |
| **01** | 1 | x | x | 1 |
| **11** | x | x | x | x |
| **10** | 1 | x | x | 1 |

KD = 1

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*Figure 3: A circuit diagram of a 4 bit synchronous BCD counter*

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*Figure 4: Waveform simulation of a 4 bit synchronous BCD counter*

**2. Discussion of used components (10) Explain each component and its implementation and give the circuit diagram.**

**AND Gate**

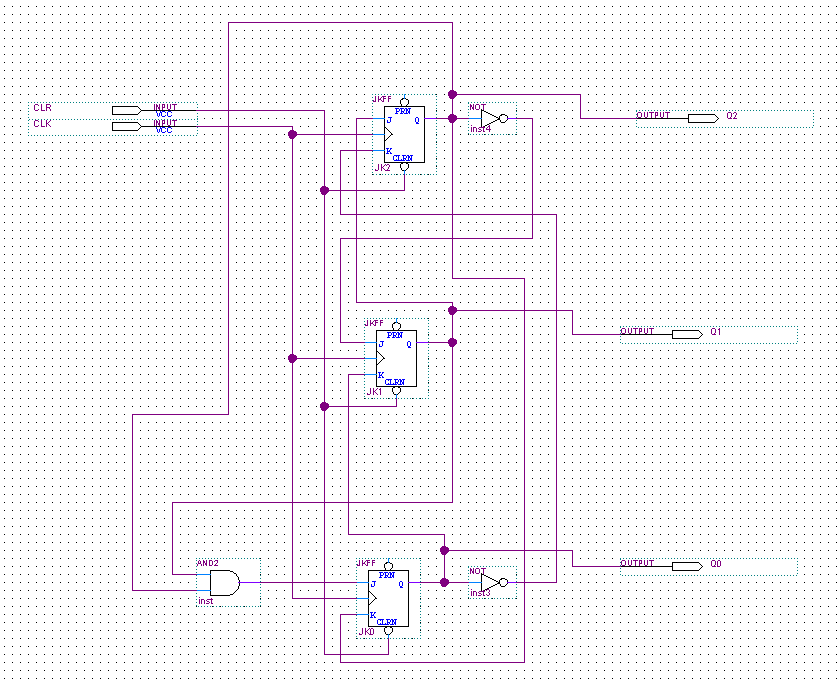
A gate where the output is 1 if and only if both inputs have a value of 1, otherwise, its output is 0.

**NOT Gate**

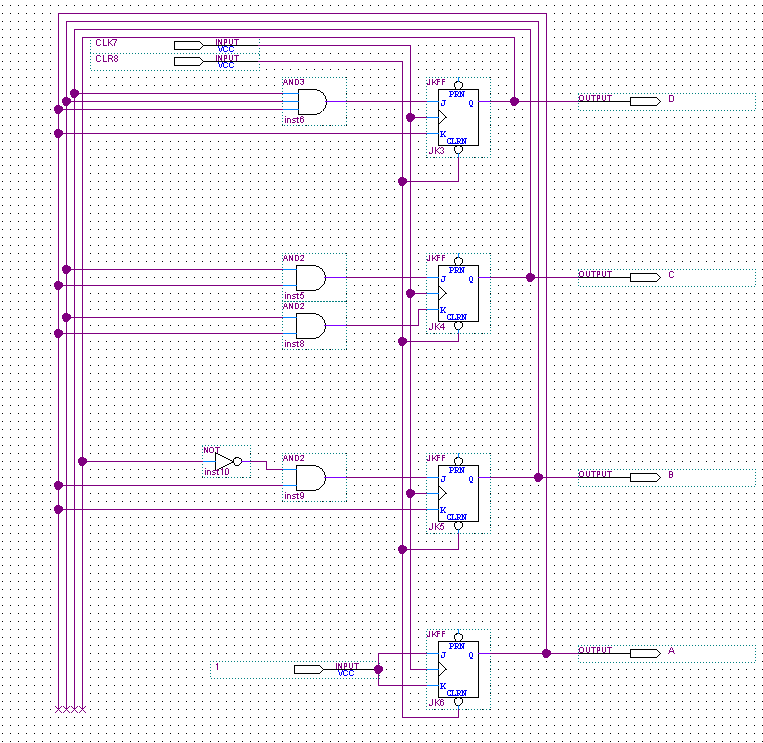
A gate where the output is 1 if the input is 0, and vice versa.

**JK Flip Flop**

It is a gated SR Flip Flop that has a clock input which prevents the invalid output when both S and R are 1

**Circuit Diagrams **

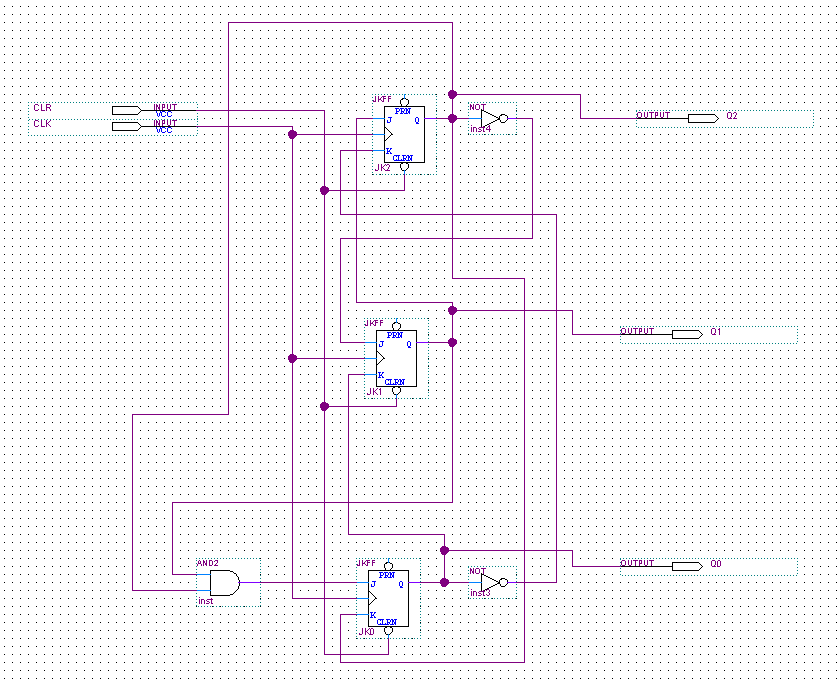
*Figure 5: A circuit diagram of a modulo 6 counter*

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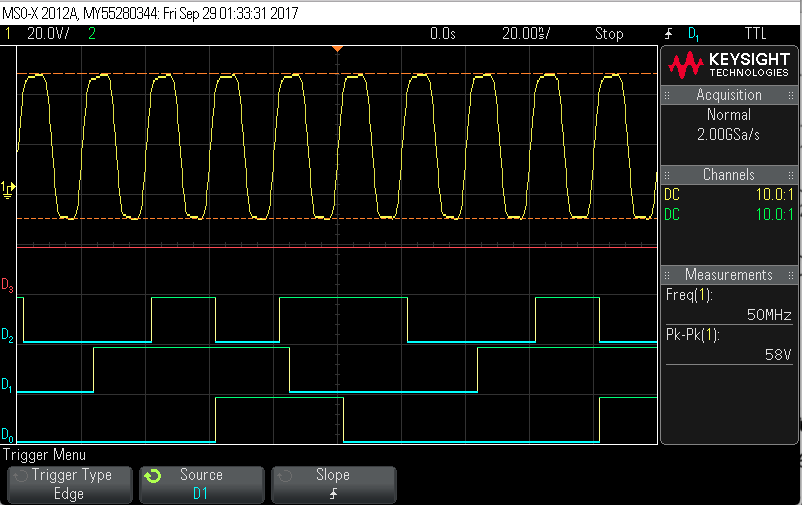
*Figure 6: A circuit diagram of a 4 bit synchronous BCD counter*

**3. Discussion of actual solution (10) Explain the actual implementation of the whole design and give the circuit diagrams.**

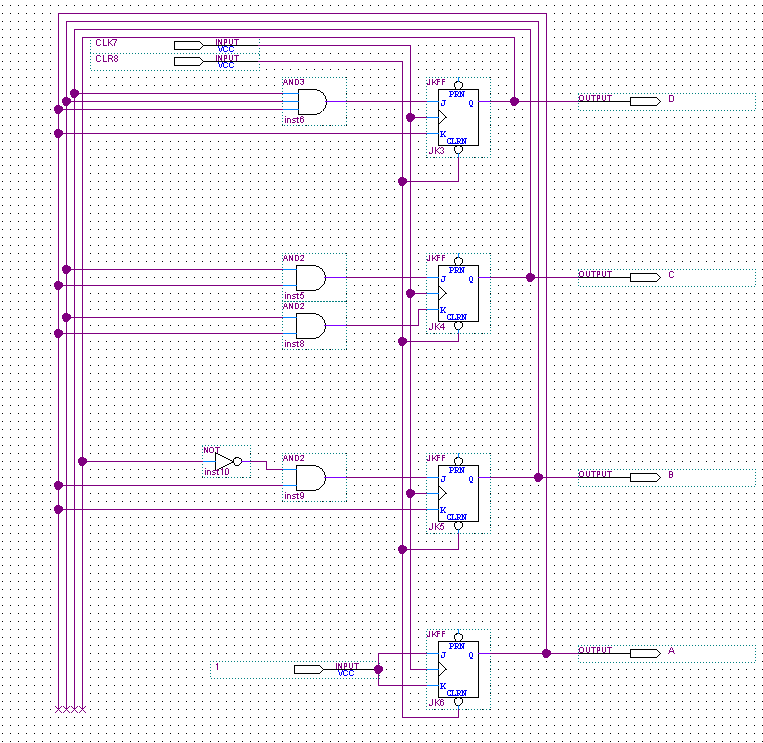
We utilized JK Flip Flops as well as a Clear and Clock input for both circuits. Furthermore, we used NOT and AND gates. The way we connected each Flip Flop corresponds to the equations we got from doing our K-Maps from the pre-lab. After we created the circuit diagrams, we uploaded the modulo 6 counter onto the Altera board. We used one of the buttons to change states, and an LED to visualize the current state. For the 4 bit BCD counter, we used the Oscilloscope to simulate and visualize what our circuit does. The result of this is shown in figure 9.

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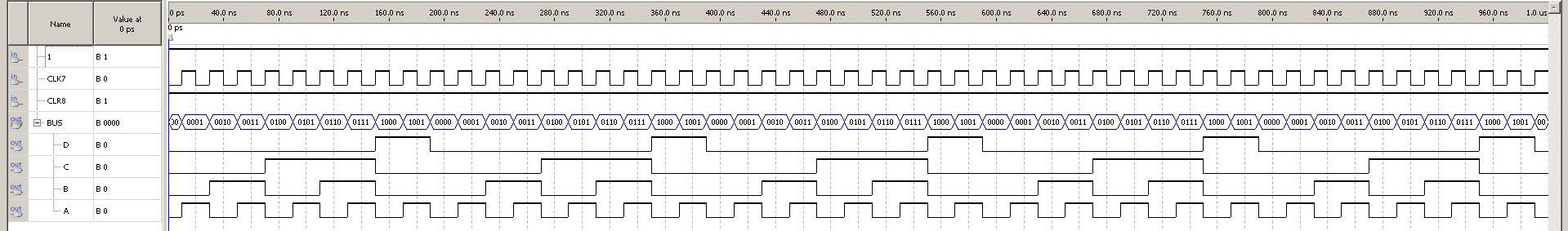
*Figure 7: A circuit diagram of a modulo 6 counter*



*Figure 9: Simulation of 3-bit synchronous BCD on the oscilloscope*

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*Figure 8: A circuit diagram of a 4-bit synchronous BCD counter*

*****Figure 9: Waveform for 4-bit synchronous BCD counter*

**4. Discussion of tool**

**Altera DE2-115 Board**

This is a circuit board which consists of multiple pins, buttons, and LEDs. It allows us to visualize and test our designed circuits from the Quartus software.

**Oscilloscope**

This is an instrument used to display and analyze the waveform of electronic signals

**Coaxial cable**

A coaxial cable conducts electrical signal using an inner conductor. We used this cable as an output for the clock from the Altera DE2-115 board to the oscilloscope.

**Ribbon cable**

A ribbon cable is a cable with many conducting wires running parallel to each other on the same flat plane. This was used to connect the Altera DE2-115 board to the oscilloscope.

**Wires**

Small wires were used to connect the two ribbon cables together

**5. Discussion of challenging problems**

We had difficulties getting the waveform simulation to display for the 4-bit synchronous BCD counter. After much effort, we got it to work.